

**Supplemental Preliminary Amendment**

Applicant: Ulrich Hachmann et al.

Serial No.: 10/592,925

(Priority Application No. DE 10 2004 012 516.3)

(International Application No. PCT/DE2005/000430)

Filed: September 14, 2006

(Priority Date: 15 March 2004)

(International Filing Date: 10 March 2005)

Docket No.: I432.135.101/P33804

Title: COMPUTER SYSTEM FOR ELECTRONIC DATA PROCESSING

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**IN THE CLAIMS**

Please cancel claim 1.

Please add claims 10-29.

1. (Cancelled)

2-9. (Cancelled)

10. (New) A computer system comprising:

a first data processing unit;

a second data processing unit;

a data transmission memory device coupled on an input side to the first data processing unit and on an output side to the second data processing unit;

wherein the data transmission memory device is configured to transmit data records from the first data processing unit to the second data processing unit;

wherein the data transmission memory device has a first memory region and a second memory region;

wherein the first memory region and the second memory region are configured to store one data record in each case; and

wherein the data transmission memory device is configured such that the transmission of a data record to be transmitted from the first data processing unit to the second data processing unit is performed in accordance with the following process:

transferring the information as to whether the second data processing unit is ready for data transmission to the data transmission memory device;

deciding, based on the information as to whether the second data processing unit is ready for data transmission, whether copying is released;

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transferring to the first memory region and storing in the first memory region the data contained in the data record to be transmitted;

copying the data record stored in the first memory region into the second memory region if copying is released; and

transferring the data record stored in the second memory region to the second data processing unit.

11. (New) The computer system of claim 10, wherein copying is released if no data is transferred from the second memory region to the second data processing unit.

12. (New) The computer system of claim 10, wherein, in the process of transferring to the first memory region and storing in the first memory region the data contained in the data record to be transmitted, only data which is not contained in the data record stored in the first memory region is transmitted.

13. (New) The computer system of claim 10, wherein the first data processing unit is a standard processor and the second data processing unit is a coprocessor, and the data to be transmitted by means of the data transmission memory device is required for the execution of a program instruction by the coprocessor.

14. (New) The computer system of claim 10, wherein the first memory region is a first memory bank and the second memory region is a second memory bank, and data is transmitted from the first memory bank into the second memory bank by means of a transfer bus.

15. (New) The computer system of claim 14, wherein the first data processing unit is connected by means of a system bus to the first memory bank, and the transfer bus has a greater bandwidth than the system bus.

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16. (New) The computer system of claim 10, wherein the data transmission memory device has a plurality of memory cells having a first memory element and a second memory element in each case, wherein each memory element is configured to store a single bit and wherein, when the data record stored in the first memory region is copied into the second memory region, the bit stored in the respective first memory element of a memory cell is copied into the respective second memory element of the memory cell by means of a local coupling.
17. (New) The computer system of claim 10, wherein both memory regions are situated on one memory chip.
18. (New) The computer system of claim 10, wherein the coprocessor is a graphics, image processing or mathematical coprocessor.
19. (New) A method for processing data comprising:
- configuring a data transmission memory device to transmit data records from a first data processing unit to a second data processing unit;
  - configuring a first memory region and a second memory region of the data transmission memory device to store one data record in each case;
  - configuring the data transmission memory device such that the transmission of a data record to be transmitted from the first data processing unit to the second data processing unit is performed in accordance with the process:
    - transferring the information as to whether the second data processing unit is ready for data transmission to the data transmission memory device;
    - deciding, based on the information as to whether the second data processing unit is ready for data transmission, whether copying is released;

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transferring to the first memory region and storing in the first memory region the data contained in the data record to be transmitted;

copying the data record stored in the first memory region into the second memory region if copying is released; and

transferring the data record stored in the second memory region to the second data processing unit.

20. (New) The method of claim 19 further comprising releasing copying if no data is transferred from the second memory region to the second data processing unit.

21. (New) The method of claim 19 further comprising transmitting only data that is not contained in the data record stored in the first memory region during the transferring to the first memory region and storing in the first memory region the data contained in the data record to be transmitted.

22. (New) The method of claim 19, wherein the first memory region is a first memory bank and the second memory region is a second memory bank, and data is transmitted from the first memory bank into the second memory bank by means of a transfer bus.

23. (New) The method of claim 19, wherein the data transmission memory device has a plurality of memory cells having a first memory element and a second memory element in each case, wherein each memory element is configured to store a single bit and wherein, when the data record stored in the first memory region is copied into the second memory region, the bit stored in the respective first memory element of a memory cell is copied into the respective second memory element of the memory cell by means of a local coupling.

24. (New) A computer system comprising:

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a first data processing unit;  
a second data processing unit; and  
a data transmission memory device having a first memory region and a second memory region each configured to store one data record in each case, the data transmission memory device coupled on an input side to the first data processing unit and on an output side to the second data processing unit,

wherein the data transmission memory device transfers a data record from the first data processing unit and stores it in the first memory region;

wherein the data transmission memory device is configured to copy the data record stored in the first memory region into the second memory region when it is determined that the second data processing unit is ready for data transmission; and

wherein the data record is transferred from the second memory region and stored in the second data processing unit.

25. (New) The computer system of claim 24, wherein the first data processing unit is a standard processor and the second data processing unit is a coprocessor, and the data to be transmitted by means of the data transmission memory device is required for the execution of a program instruction by the coprocessor.

26. (New) The computer system of claim 24, wherein the first memory region is a first memory bank and the second memory region is a second memory bank, and data is transmitted from the first memory bank into the second memory bank by means of a transfer bus.

27. (New) The computer system of claim 26, wherein the first data processing unit is connected by means of a system bus to the first memory bank, and the transfer bus has a greater bandwidth than the system bus.

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28. (New) The computer system of claim 24, wherein the data transmission memory device has a plurality of memory cells having a first memory element and a second memory element in each case, wherein each memory element is configured to store a single bit and wherein, when the data record stored in the first memory region is copied into the second memory region, the bit stored in the respective first memory element of a memory cell is copied into the respective second memory element of the memory cell by means of a local coupling.

29. (New) The computer system of claim 24, wherein both memory regions are situated on one memory chip.